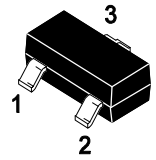
LP3401LT1G

30V P-Channel Enhancement-Mode MOSFET

1. FEATURES

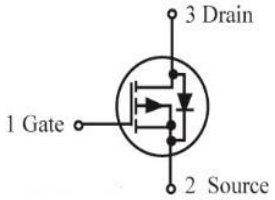
- VDS = -30V
- RDS(ON) ≤ 70mΩ (VGS = -10V)
- RDS(ON) ≤ 80mΩ (VGS = -4.5V)
- RDS(ON) ≤ 120mΩ (VGS = -2.5V)
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



SOT23(TO-236)

2. APPLICATIONS

- Advanced trench process technology
- High density cell design for ultra low on-resistance.



3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP3401LT1G	A1	3000/Tape&Reel
LP3401LT3G	A1	10000/Tape&Reel

4. MAXIMUM RATINGS(Ta = 25ºC)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDSS	-30	V
Gate–to–Source Voltage – Continuous	VGS	±12	V
Drain Current – Continuous TA = 25°C(Note 1) – Pulsed (Note 2)	 ID IDM	 -4.2 -30	A

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Power Dissipation(Note 1)	PD	1.4	W
Thermal Resistance, Junction–to–Ambient(Note 1) Junction–to–Case	 RΘJA RΘJC	 125 100	ºC/W
Junction and Storage temperature	TJ,Tstg	−55~+150	ºC

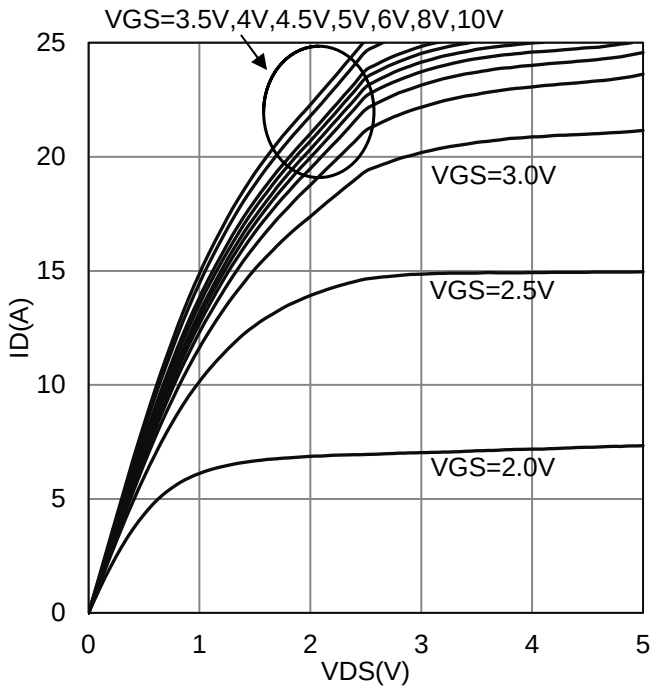
1.Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu.
2.Pulse width limited by maximum junction temperature

6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

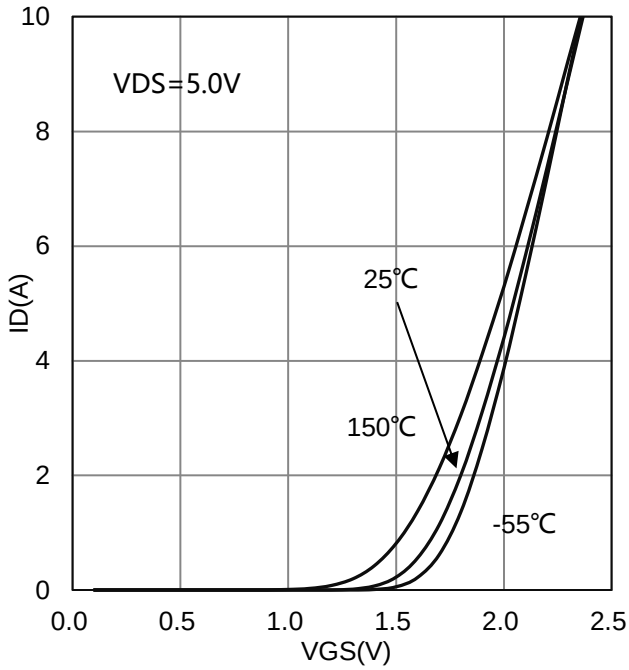
Characteristic		Symbol	Min.	Typ.	Max.	Unit
STATIC						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)		VBRDSS	-30	-	-	V
Gate-Source Threshold Voltage (VDS =VGS , ID =-250μA)		VGS(th)	-0.6	-1.0	-1.3	V
Gate-Body Leakage Current (VDS =0V, VGS =± 12V)		IGSS	-	-	± 100	nA
Zero Gate Voltage Drain Current (VDS = -24 V, VGS = 0 V)		IDSS	-	-	-1	μA
Drain-Source On-Resistance(Note 3) (VGS = -10 V, ID = -4.2 A) (VGS = -4.5 V, ID = -4 A) (VGS = -2.5 V, ID = -1 A)		RDS(ON)	- - -	- - -	70 80 120	mΩ
Diode Forward Voltage(Note 3) (IS = -1 A, VGS = 0 V)		VSD	-	-0.75	-1.3	V
DYNAMIC						
Total Gate Charge	(VDS = -15 V, VGS = -4.5 V,ID = -4 A)	Qg	-	7.4	-	nC
Gate-Source Charge		Qgs	-	1.3	-	
Gate-Drain Charge		Qgd	-	2.6	-	
Turn-On Delay Time	(VDS = -15 V, RL = 3.6 Ω, VGS= -10V, RGEN =6.2 Ω)	td(on)	-	2.6	-	ns
Rise Time		tr	-	10	-	
Turn-Off Delay Time		td(off)	-	52	-	
Fall Time		tf	-	16.2	-	
Input Capacitance	(VDS = -15 V, VGS = 0 V, f = 1 MHz)	Ciss	-	740	-	pF
Output Capacitance		Coss	-	51	-	
Reverse Transfer Capacitance		Crss	-	44	-	
Gate Resistance (VDS=0V ,VGS=0V, f=1.0MHz)		Rg	-	8.5	-	Ω

3.Pulse test; pulse width≤300μs, duty cycle≤ 2%

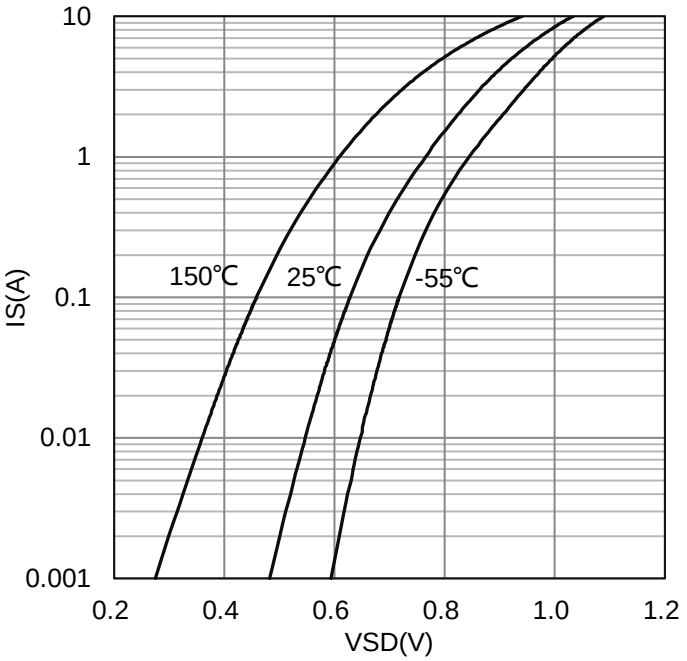
7. ELECTRICAL CHARACTERISTICS CURVES



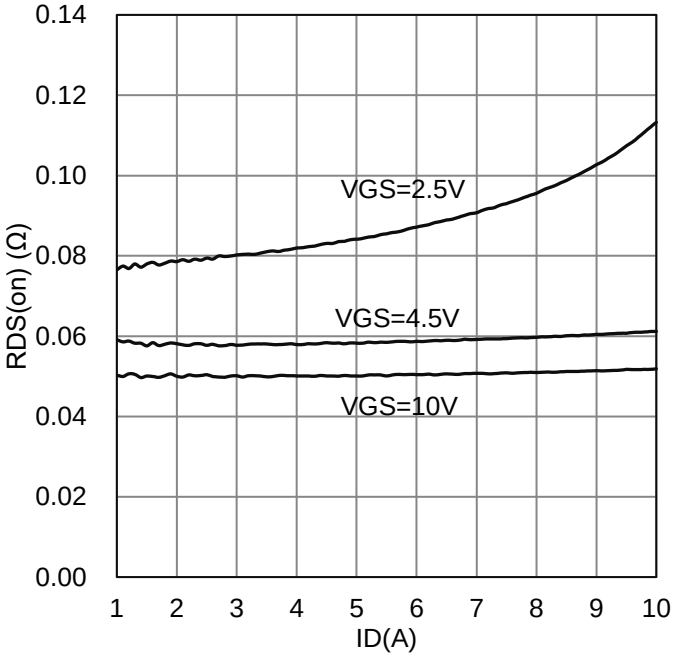
ID vs. VDS



ID vs. VGS

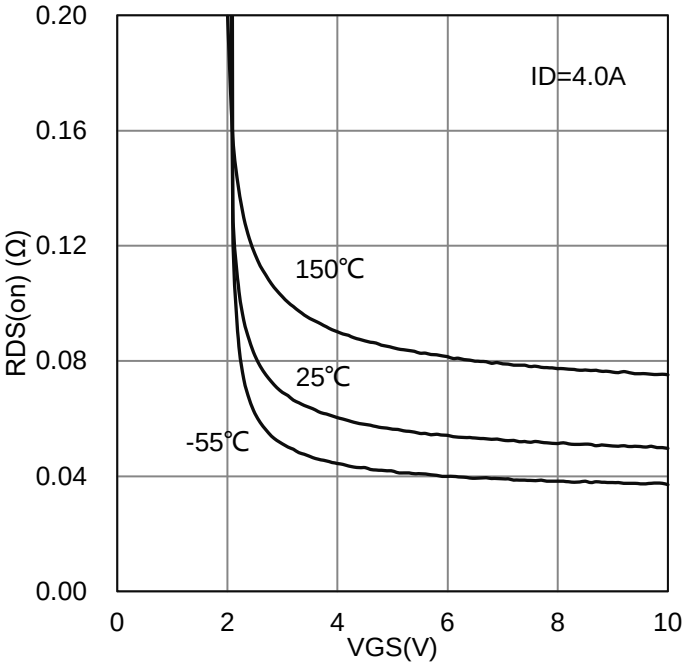


IS vs. VSD

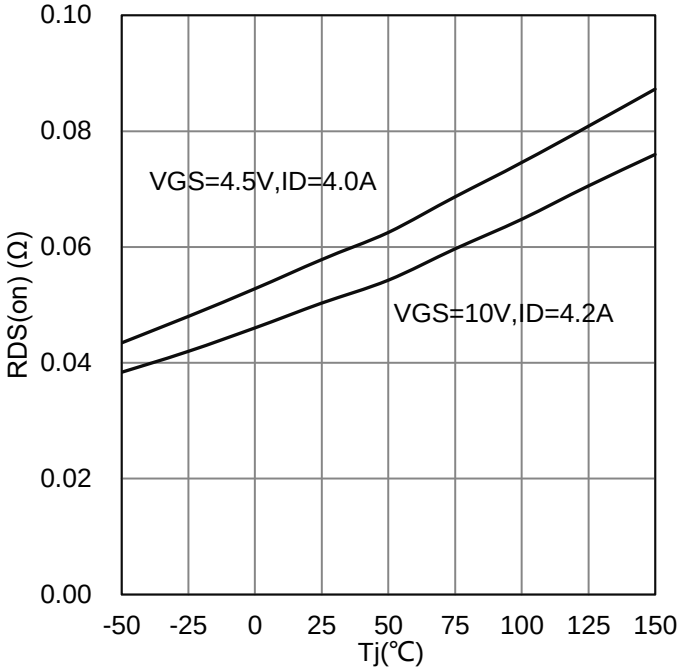


RDS(on) vs. ID

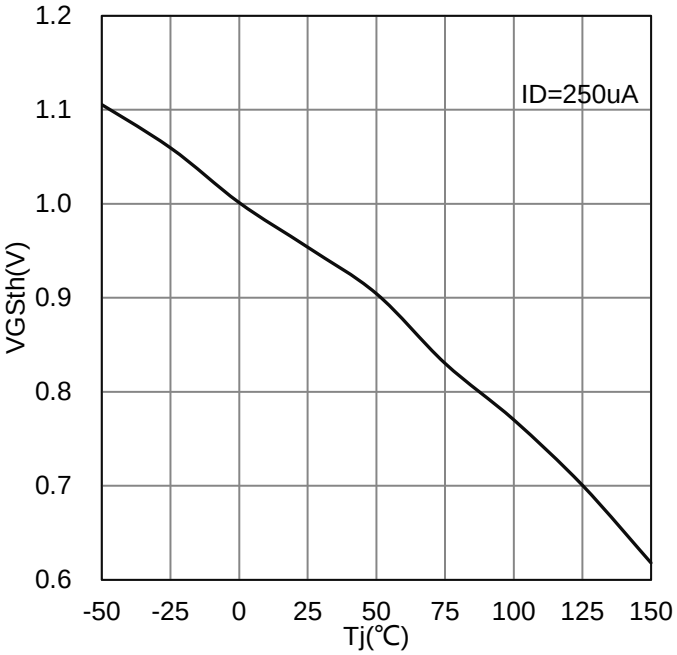
7. ELECTRICAL CHARACTERISTICS CURVES(Con.)



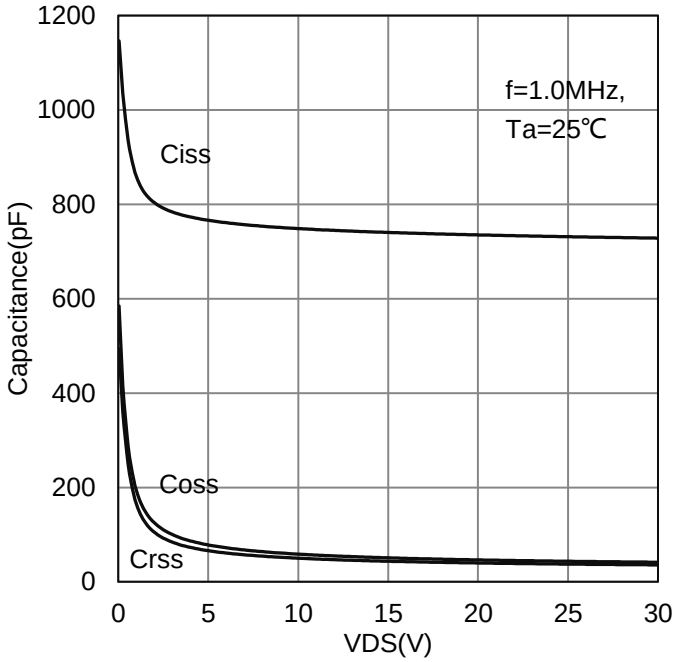
RDS(on) vs. VGS



RDS(on) vs. Tj

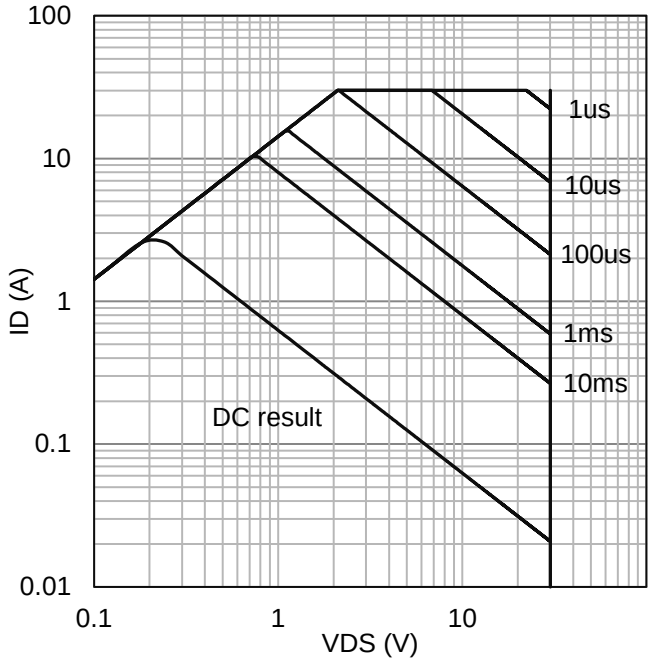


VGSth vs. Tj



Capacitance

7. ELECTRICAL CHARACTERISTICS CURVES(Con.)

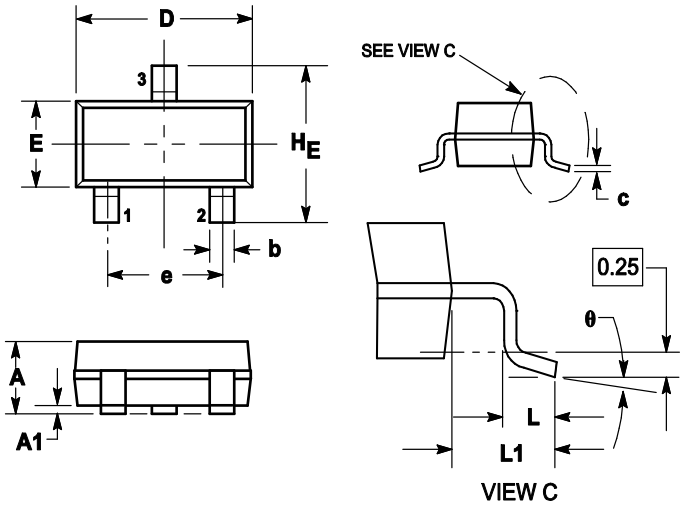


Safe Operating Area

8.OUTLINE AND DIMENSIONS

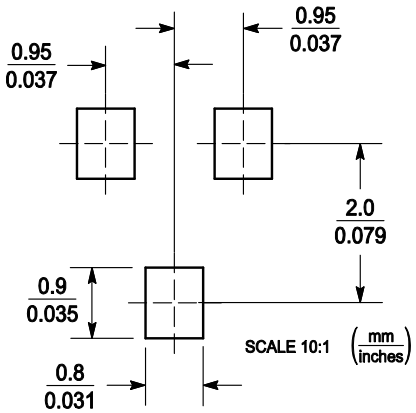
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
H_E	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9.SOLDERING FOOTPRINT



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